AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 12-20 without prejudice. Please add new claims 21-29.

1. (CURRENTLY AMENDED) A method for ~~modeling analog signals~~ verification, comprising the steps of:

(A) generating ~~detecting~~ one or more ~~attributed~~ analog signals utilized by an analog design; ~~and~~

(B) generating one or more source signals by adding a digital signature to each of said analog signals; and

(C) modeling said ~~attributed~~ analog design ~~signals by adding a signature to each of~~ using said ~~one or more attributed~~ source signals in place of said analog signals for verifying connectivity.

2. (CURRENTLY AMENDED) The method according to claim 1, wherein step ~~(B)~~ (C) further comprises the step of:

performing ~~digital~~ one or more simulations of said analog design with said ~~one or more attributed analog~~ source signals propagating through said analog design.

3. (CURRENTLY AMENDED) The method according to claim 1, wherein each of said ~~one or more~~ digital signatures corresponds to a type of said analog signals having a predetermined parameter.

4. (CURRENTLY AMENDED) The method according to claim 1, wherein each of said ~~one or more~~ digital signatures comprises ~~an~~ a unique pulse width ~~digital signature~~.

5. (CURRENTLY AMENDED) The method according to claim 1, ~~wherein step (B)~~ further ~~comprises~~ comprising the step of:

performing verification of said ~~one or more attributed~~ analog design ~~signals~~.

6. (CURRENTLY AMENDED) The method according to claim ~~1~~2, wherein ~~step (B)~~ performing said simulations further comprises the sub-step of:

verifying ~~determining~~ a connectivity of said ~~one or more attributed~~ analog signals through said analog design.

7. (CURRENTLY AMENDED) The method according to claim ~~1~~ 2, wherein ~~step (B)~~ performing said simulations further comprises the sub-step of:

verifying a model of an analog block within said analog design configured to receive at least a particular one of said ~~one or more attributed~~ analog signals.

8. (CURRENTLY AMENDED) The method according to claim 7, wherein ~~step (B)~~ verifying said model further comprises the sub-step of:

verifying ~~a second one or more models~~ an output signal of said analog block for said digital signature associated with said particular one of said ~~blocks configured to receive another at least one of said one or more attributed~~ analog signals.

9. (CURRENTLY AMENDED) A method for testing a model of ~~a~~ an analog device, comprising the steps of:

(A) generating one or more attributed signals each (i) having a unique digital signature and (ii) presented by a source block within ~~performing tests on~~ said model of said analog device; and

(B) verifying connectivity of ~~one or more~~ said attributed ~~analog~~ signals to a destination block within said model of said analog device by verifying ~~one or more~~ reception of said unique digital signatures associated with each of said ~~one or more~~ attributed ~~analog~~ signals at said destination block.

10. (CURRENTLY AMENDED) The method according to claim 9, ~~wherein step (B) further comprises~~ further comprising the step of:

disabling processing of a particular one of said attributed signals if said ~~one or more attributed analog signals are~~ particular signal is not verified at said destination block~~, disabling said device~~.

11. (CURRENTLY AMENDED) The method according to claim 9, ~~wherein step (B)~~ further ~~comprises~~ comprising the step of:

verifying a model of ~~an analog~~ said destination block configured to receive at least one of said ~~one or more~~ attributed ~~analog~~ signals.

12. (CANCELED)

13. (CANCELED)

14. (CANCELED)

15. (CANCELED)

16. (CANCELED)

17. (CANCELED)

18. (CANCELED)

19. (CANCELED)

20. (CANCELED)

21. (NEW) The method according to claim 1, wherein each of said digital signatures comprises a plurality of pulses.

22. (NEW) The method according to claim 1, wherein each of said digital signatures comprises a varying frequency signal.

23. (NEW) A system comprising:

a source for a plurality of signals, at least one of said signals representing an analog signal having a digital signature; and

a simulator connected to said source and configured to (i) simulate an analog design, (ii) receive said signals and (iii) verify a connectivity of said analog signal in said analog design using said digital signature.

24. (NEW) The system according to claim 23, wherein said source comprises an analog source block configured to generate said analog signal.

25. (NEW) The system according to claim 24, wherein said source further comprises an adder block configured to (i) generate said digital signature and (ii) add said digital signature to said analog signal.

26. (NEW) The system according to claim 25, wherein said source further comprises a digital source block configured to generate at least one of said signals representing a digital signal.

27. (NEW) The system according to claim 23, wherein said digital signature comprises a plurality of pulses.

28. (NEW) The system according to claim 27, wherein said pulses have a unique width to identify said analog signal.

29. (NEW) The system according to claim 27, wherein said digital signature has a varying frequency.